

Dario Aro
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Amerson
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pan et al.

Serial No.: TO BE ASSIGNED

Filed: May 6, 1998

**For: TECHNIQUE FOR ELIMINATION OF
PITTING ON SILICON SUBSTRATE
DURING GATE STACK ETCH**

Examiner: TO BE ASSIGNED

Group Art Unit: TO BE ASSIGNED

**Attorney Docket No.: 2915.1US
(96-0149.01)**

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

DOCUMENTS

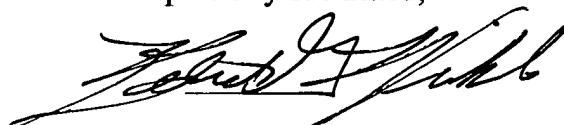
U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventor</u>
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Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Information Disclosure Statement is filed concurrent with the filing of the above-identified application, thus no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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